## MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE

(UGC-AUTONOMOUS INSTITUTION)

Affiliated to JNTUA, Ananthapuramu & Approved by AICTE, New Delhi NAAC Accredited with A+ Grade, NIRF India Rankings 2024 - Band: 201-300 (Engg.) NBA Accredited - B.Tech. (CIVIL, CSE, CST, ECE, EEE, MECH), MBA & MCA www.mits.ac.in

## **EXAM SECTION - NOTIFICATION DATE: 05.12.2024**

## M. Tech I Year I Semester I Mid - Term Test Schedule December- 2024

Academic Year - 2024 - 25

Timings: FN: 09:30 AM to 11:30 AM AN: 03.00 PM to 05.00 PM

PRINCIPAL

Principal

Madanapalle Institute of

Technology & Science

MADANAPALLE

| DATE / DAY/SESSION        |    | VLSI & EMBEDDED Systems   |
|---------------------------|----|---|
| 16.12.2024<br>(Monday)    | FN | CMOS Digital IC Design- 24VESP101   |
|                           | AN | Microcontrollers and Programmable Digital Signal Processors-<br>24VESP102 |
| 17.12.2024<br>(Tuesday)   | FN | FPGA Architectures and Applications-24VESP403                             |
|                           | AN | Low Power VLSI Design-24VESP404   |
| 18.12.2024<br>(Wednesday) | FN | Research Methodology and IPR-24RMP101                                     |
|                           | AN | Disaster Management-24AUP901  |

Note: 1. HOD is requested to circulate among the faculty in the department.

Controller of Examinations

CONTRULLER OF EXAMINATIONS WEODY TO:

1. HOD

2. TI Road angul

3. Copy to HOD to be read in M. Tech, I Year I Semester Class Room

4. Notice Board (AS & Dept)

5. File (AS)

E Copy To: Vice Principal (Academics) Vice Principal (Administration) HOD SAO (G) PRO

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